REMARKS:

Applicants have carefully studied the Supplemental Final Examiner's Action and all references cited therein. These explanatory remarks are believed to be fully responsive to the Action. Accordingly, this important patent application is now believed to be in condition for allowance.

Applicants respond to the outstanding Action by centered headings that correspond to the centered headings employed by the Office, to ensure full response on the merits to each finding of the Office.

Claim Rejections – 35 U.S.C. § 103(a)

In response to the Applicant's assertion that in the Final Office Action mailed on June 20, 2007, the rejection of independent claim 25 was improper for failing to fully address the claimed limitations, the Examiner has withdrawn the rejection of claim 25, and a new rejection of claim 25 has been set forth in the Supplemental Office Action, under the same grounds 35 U.S.C § 103(a) as being unpatentable over Koschella (U.S. Patent No. 7,054,121) in view of Desmicht et al. (US 20060156033), for the purpose of further clarifying the rejection of the claimed limitations of the Final Office Action.

Applicants acknowledges the quotation of 35 U.S.C § 103(a).

Claim 25 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Koschella (U.S. Patent No. 7,054,121) in view of Desmicht et al. (US 20060156033).

Regarding independent claim 25, the Office states that Koschella discloses a processor-memory system with a protection circuit, Fig. 1, comprising: A memory (memory device 3) including a protected area (B0, B1, Bi, .. Bn), which is protected by a protection circuit 1, in the event of an unauthorized external memory access; "a JTAG interface clocked by a JTAG clock signal received from an external JTAG hardware", such as an externally accessible interface 6, which is a standard Joint Test Action Group (JTAG) interface. The data can also be read as data d1 at the externally accessible data interface 6 or written from there into the memory device 3, Fig. 1; a JTAG clock signal (TCK) in inherently part of JTAG IEEE Standard 1149.1 signals including (TMS, TCK,

TDI, and TDO), which are normally provided from an external test system compliant with standard IEEE 1149.1 JTAG interface; "a controller configured to allow said external JTAG hardware to write information into said non-volatile memory through said JTAG interface, wherein said controller is clocked either by a system clock signal or by said JTAG clock signal if said system clock signal is not available", such as (logic device 5.1) Fig. 4 and Fig. 6, which allows the external test system compliant with standard IEEE 1140.1 JTAG interface to write (data d1) into the memory device 3. The controller is closed by a system clock signal write clock, which is a register write enable signal WE_{MPCR} from the CPU 2, which generates the read signal $RE_{memory\ i}$ or write enable signal $WE_{memory\ i}$, respectively, for reading or writing in the selected memory area, Fig. 6.

Additionally, the Office states that the recited limitation, "or by said JTAG clock signal if said system clock signal is not available", is in the alternative format, and therefore it has not been given patentable consideration and that therefore, only the limitation, "said controller is clocked by a system clock signal", has been given patentable consideration.

Applicant respectfully disagrees with the finding by the Office based on the following enumerated grounds.

1. The Applicant contends that the response presented by the Office is improper, because if the Office believed that the alternative language of claim 25, caused the claim to not particularly point out and distinctly define the metes and bounds of the subject matter that would be protected by the patent grant, a rejection under 35 U.S.C. 112, second paragraph, should have been issued. Alternatively, if the Office believed that the alternatives presented in the claim were somehow independent and distinct, then a restriction requirement under 35 U.S.C. 121 should have been issued, prior to further prosecution of the claims. Applicant requests that the Office make the necessary correction to the Supplemental Office Action in accordance with the U.S. Patent Laws.

2. The Office states that patentable weight is only being given to the claim limitation which states, "said controller is clocked by a system clock signal", and not to the claim limitation which states, "or by said JTAG clock signal if said system clock signal is not available". Applicant contends that it is the responsibility of the examining Office to address each claim limitation for patentability. The decision by the Office to not afford patentable weight to the claim limitation which states, "or by said JTAG clock signal if said system clock signal is not available", is believed to be improper and such a decision is not supported by U.S. Patent Laws or the M.P.E.P. Applicant does not believe that the use of alternative format in the language of claim 25 allows the Office to only give patentable weight to the claim limitations he/she chooses. Accordingly, Applicant requests that the Office withdraw the statement and afford patentable weight to all the limitations of claim 25.

3. It is well established that the metes and bounds of claims are not rendered unclear merely because of the presence of alternative language in the claims[1]. Alternative expressions are generally permitted if such expressions introduce no uncertainty or ambiguity with respect to claim scope or clarity. More specifically, alternative expressions using the word "or" may also be acceptable and may not be in violation of Section 112, second paragraph. The alternative expression of claim 25 states, "said controller is clocked either by a system clock signal or by a JTAG clock signal if said system clock signal is not available". Applicant believes that the language of the claims does not introduce any uncertainty or ambiguity with respect to the claim scope or clarity. It is clear from this limitation that if the system clock is available, the controller is closed by the system clock, and if the system clock is unavailable, the controller is clocked by the JTAG clock signal. As such, Applicant contends that the alternative language in claim 25 is permissible and that all the limitations in claim 25 should be afforded patentable weight.

Assuming that the alternative expression of claim 25 which states, "said controller is clocked either by a system clock signal or by a JTAG clock signal if said system clock signal is not available", is given the appropriate patentable weight by the Office, claim 25

[1] *Ex parte* Wu, 10 USPQ 2d 2031, 2032 (B.P.A.I. 1989); *Ex parte* Cordova, 10 USPQ 2d 1949, 1950 (B.P.A.I. 1987)

positively recites a controller configured to allow said external JTAG hardware to write information into said non-volatile memory through said JTAG interface, wherein said controller is clocked either by a system clock signal or by a JTAG clock signal if said system clock signal is not available. As such, the controller allows the external JTAG hardware to write information into the non-volatile memory prior to the boot-up of the CPU that provides the system clock signal.

Applicant contends that neither Koschella or Desmicht et al. describe a JTAG interface clocked by a JTAG clock signal received from an external JTAG hardware and a controller configured to allow said external JTAG hardware to write information into said non-volatile memory through said JTAG interface, wherein said controller is clocked by said JTAG clock signal if said system clock signal is not available as disclosed and claimed by the present invention.

The Office states in the Supplemental Final Office Action that the claim limitation of claim 25 which includes, "the controller is clocked by the JTAG clock signal", is taught by Koschella, wherein Koschella discloses JTAG signals coupled to the inputs of the AND gate 14, which include a (TCK) clock for clocking the controller, as shown in Fig. 6.

Applicant respectfully disagrees with this finding by the Office.

As described in paragraph [0023] of the instant invention, in normal operation, the controller 102 is clocked by the system clock signal generated by the clock generator 110. Since the JTAG I/F 103 is clocked with a JTAG clock signal provided by the JTAG H/W 122, a first input buffer 111 is used in a conventional fashion to synchronize the signals from the JTAG I/F 103 with signals in the controller 105. As such, the present invention makes it clear that both JTAG clock signals and system clock signals may be present in the system and that these clock signals may be synchronized.

The Office contends that Koschella discloses at Fig. 6, JTAG signals coupled to the inputs of the AND gate 14, which include a (TCK) clock for clocking the controller. The Office previously identified the "controller" as logic device 5.1 of Koschella. Fig. 6 illustrates the logic device 5.1 from Fig. 4 in more detail. As can easily be seen from Fig. 4, the inputs to logic device 5.1 are RC, WE and OPC, all of which originate at the CPU. As such, Applicant fails to see where Koschella illustrates a clock for clocking the controller that originates from the JTAG interface.

Additionally, throughout the detailed description regarding Fig. 6, Koschella discusses the clock signal being initiated from the CPU. More specifically, Koschella states at col. 5, lines 54-55, "the write clock is a register write enable signal WE_{MPCB} from the CPU 2", and at col. 5, lines 66-67, "the D flip-flop 11 is clocked with the op-code fetch signal OPC at the C input". As such, Koschella does not illustrate or describe a controller that is clocked by said JTAG clock signal if said system clock signal is not available as disclosed and claimed by the present invention.

For the reasons cited above, Applicant believes that claim 25 is patentable over Koschella in view of Desmicht and is believed to be in condition for allowance.

ADDITIONAL REMARKS

As previously argued, Applicant believes that the alternative language of claim 25 is proper and that the claim is patentable as it stands. However, in order to further the prosecution of the claims in this case, the Applicant would be willing to amend claim 25 to remove the alternative format language if such an amendment would place claim 25 in condition for allowance.

CONCLUSION

Applicants respectfully request reconsideration of the Application based on the amendments and remarks presented above. In light of the above amendments and remarks, Applicants respectfully assert that the claims now pending in the Application are in condition for allowance.

Applicants have made a diligent effort to place the claims in condition for allowance. Should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicants' representative, Kenneth Glass, at (408) 354-4448 so that such issues may be resolved as expeditiously as possible.

For the reasons set forth in this paper, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

9/21/07
(Date)

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